

VB125SP

HIGH VOLTAGE IGNITION COIL DRIVER POWER IC

TARGET DATA

1/8

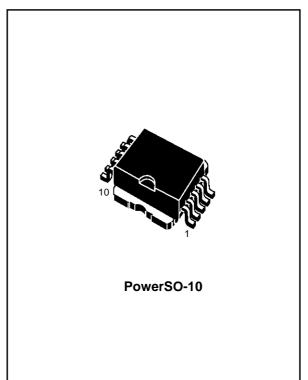
TYPE	V _{CL}	I _{CL}	I _{CC}
VB125SP	370 V	9 A	200 mA

- PRIMARY COIL VOLTAGE INTERNALLY SET
- COIL CURRENT LIMIT INTERNALLY SET
- LOGIC LEVEL COMPATIBLE INPUT
- BATTERY OPERATION
- SINGLE FLAG-ON COIL CURRENT
- TEMPERATURE COMPENSATED HIGH VOLTAGE CLAMP

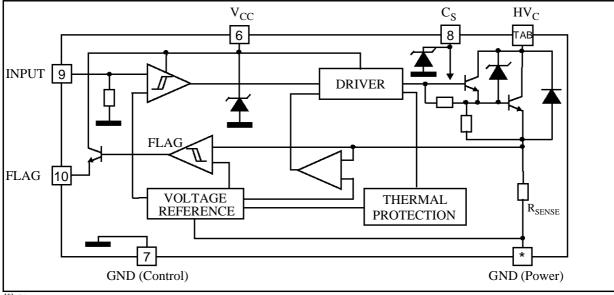
DESCRIPTION

The VB125SP is a high voltage power integrated circuit made using SGS-THOMSON Microelectronics Vertical Intelligent Power Technology, with vertical current flow power darlington and logic level compatible driving circuit.

The VB125SP can be directly biased by using the 12V battery voltage, thus avoiding to use a low voltage regulator. It has built-in protection circuits for coil current limiting and collector voltage clamping. It is suitable as smart, high voltage, high current interface in advanced electronic ignition system.



BLOCK DIAGRAM



(*) Pins 1...5

September 1997

This is preliminary information on a new product in development or undergoing evaluation. Details are subject to change without notice.

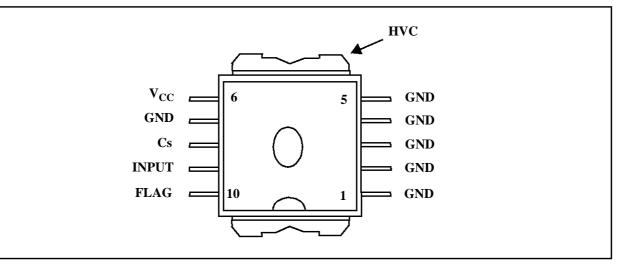
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit V	
ΗV _C	Collector Voltage (Internally Limited)	-0.3V to V _{CLAMP}		
۱ _C	Collector Current (Internally Limited)	10	А	
V _{CC}	Driving Stage Supply Voltage	-0.2 to 40	V	
I _{CC}	Driving Circuitry Supply Current	400	mA	
۱ _S	Logic Circuitry Supply Ccurrent	100	mA	
V _{IN}	Input Voltage	-0.3 to 6	V	
P _{TOT}	Power Dissipation	TBD	W	
V _{ESD}	ESD Voltage (HVC Pin)	-4 to 4	KV	
V _{ESD}	ESD Voltage (Other Pin)	-2 to 2	KV	
Тj	Operating Junction Temperature	-40 to 150	°C	
T _{STG}	Storage Temperature Range	-55 to 150	°C	

THERMAL DATA

R _{thj-case}	Thermal Resistance Junction - Case	MAX	1.2	°C/W
R _{thj-amb}	Thermal Resistance Junction - Ambient	MAX	62.5	°C/W

CONNECTION DIAGRAM



PIN FUNCTION

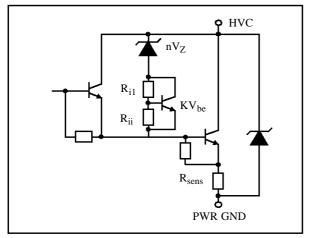
No	Name	FUNCTION
1-5	GND	Emitter Power Ground
6	V _{CC}	Logic Supply Voltage
7	GND	Control Ground (*)
8	C _S	Logic Level Supply Voltage Filter Capacitor
9	INPUT	Logic Input Channel
10	FLAG	Diagnostic Output Signal
TAB	HVC	Primary Coil Output Driver

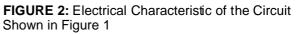
(*) Pin 6 must be connected to pins 1-5 externally

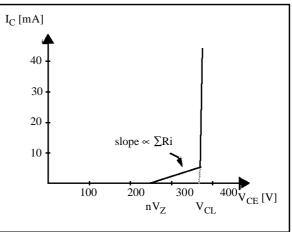
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{CL}	High Voltage Clamp	I _C = 6.5 A; (See Note 2)	340	370	400	V
V _{CE(sat)}	Saturation Voltage of the Power Stage	$I_C = 5A; V_{in} = 4V$ (See Note 3)			2	V
	Power Off Supply Current	V _{in} =0.4V V _{bat} = 14V(Notes 4-5)			20	mA
I _{CC(off)}		$V_{in}=0.4V$ $V_{bat}=24V$			80	mA
	Power On Supply Current	$V_{ln} = 4 V V_{bat} < 14V (Note 4-5)$			220	mA
I _{CC(on)}		$V_{in} = 4 V$ $V_{bat} = 24 V$			300	mA
I _{CL}	Coil Current Limit	V _{in} = 4 V (See Note 6-7)	8		10	А
V _{inH}	High Level Input Voltage		4			V
V _{inL}	Low Level Input Voltage				0.8	V
V _{IN(hyst.)}	Input Hysteresis Voltage		0.4			V
l _{inH}	High Level Input Current	$V_{in} = 4 V$	10		150	μA
l _{inL}	Low Level Input Current	V _{in} = 0.8 V			-100	μA
V_{diagH}	High Level Diagnostic Output Voltage	$\begin{array}{ll} R_{EXT} = 22 \ K \ \Omega & C_{EXT} = 1 \ nF \\ (\text{See Note 8}) \end{array}$	3.5		5.5	V
V_{diagL}	Low Level Diagnostic Output Voltage	$\begin{array}{ll} R_{EXT} = 22 \ K \ \Omega & C_{EXT} = 1 \ nF \\ (\text{See Note 8}) \end{array}$			0.5	V
I _{diagTH}	Current Threshold Level Diag- nostic	$T_j = 25 ^{\circ}C$ (See Note 7and fig. 5)	4.25	4.5	4.75	А
l _{diag}	High Level Flag Output Current	I _C >I _{DiagTH} (See Note 7)	0.5			mA
I _{diag(leak)}	Leakage Current on Flag Output	V _{in} = LOW			10	μΑ
V _F	Antipallel Diode Forward Voltage	I _C = -1 A			2	V
E _{s/b}	Single Pulse Avalanche Energy		300			mJ
Τ _j	Thermal Output Current Control	IN = ON (See Note 9)	150			°C
t _{d(on)}	Turn-on Delay Time of Output Current	(See Note 10)		TBD		μs
t _{d(off)}	Turn-off Delay Time of Output Current	(See Note 11)		TBD		μs
t _{d(off)}	Turn-off Delay Time of Output Current	(See Note 11)		TBD		μs

ELECTRICAL CHARACTERISTICS (V_{bat} = 6 to 24V; -40°C<T_j<125°C; R_{coil} = 400 to 700m Ω ; L_{coil} = 2 t@mH; unless otherwise specified; See Note 1)

FIGURE 1: Temperature Compensated High Voltage Clamp









NOTE 1 Parametric degradation are allowed with $6V < V_{bat} < 10V$ and $V_{bat} > 24V$.

NOTE 2 In the high voltage clamping structure of this device a temperature compensation has been implemented. The circuit schematic is shown in fig. 1. The KVbe cell takes care of the temperature compensation. The whole electrical characteristic of the new circuit is shown in fig. 2. Up to $V_{CE}=nV_Z$ no current will flow into the collector (just the leakage current of the power stage); for $nV_Z < V_{CE} < V_{CL}$ a current begins to flow across the resistances of the KVbe compensation circuit (typical slope \cong 20 K Ω) as soon as the Vcl is reached the dinamic resistance drop to ~4 Ω to protect the device against overvoltage (See Fig. 3).

NOTE 3 The saturation voltage of the Power stage includes the drop on the sensing resistor.

NOTE 4 Considering the different ways of operation of the device (with or without spark, etc...) there are some short periods of time in which the output terminal (HV_C) is pulled below ground by a negative current due to leakage inductances and stray capacitances of the ignition coil. With VIPower devices, if no corrective action is taken, these negative currents can cause parasitic glitches on the diagnostic output. To kill this potential problem, a circuit that avoids the possibility for the HV_C to be pulled undeground, by sending the required negative current from the battery is implemented in the VB125SP.For this reason there are some short periods in which a current exceeding 220 mA flows in the pin V_D .

NOTE 5 A zener protection of 16V (typical) is placed on the supply pin (V_{CC}) of the chip to protect the internal circuitry. For this reason, when the battery voltage exceedes that value, the current flowing into V_{CC} pin can be greater than the maximum current specified at V_{bat} =14V (both in power on and power off condictions) : it will be limited by an internal resistor.

NOTE 6 The primary coil current value IcI must be measured 1 ms after desaturation of the power stage.

NOTE 7 These limits apply with regard to the minimum battery voltage and resistive drop on the coil and cables that permit to reach the limitation or diagnostic level.

NOTE 8 No internal Pull-Down.

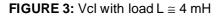
NOTE 9 Tjmin= 150 °C means that the behaviour of the device will not be affected for junction temperature lower than 150 °C. For higher temperature, the thermal protection circuit will begin its action reducing the lcl limit according with the power dissipation. Chip temperature is a function of the Rth of the whole system in which the device will be operating (See Fig.4).

NOTE 10 Propagation Time measured from input voltage rising edge to 50% of output voltage falling edge.

NOTE 11 As soon as the input signal is switched low the stored charges in the base of the power transistor are removed and the so called «Turn-off Delay Time of Coil Current» begins; after at the «Turn-off Fall Time of Coil Current» starts and, at the same time, the HVC rises.

tdLH is defined as the time between the negative edge of the input pulse to the point where the HVC reaches 100V. tfLH is defined as the delay between the 90% and the 10% of the coil current.

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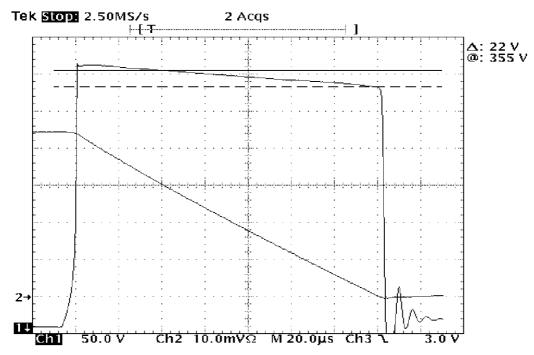


FIGURE 4: Output Current Waveform after Thermal Protection Activation.

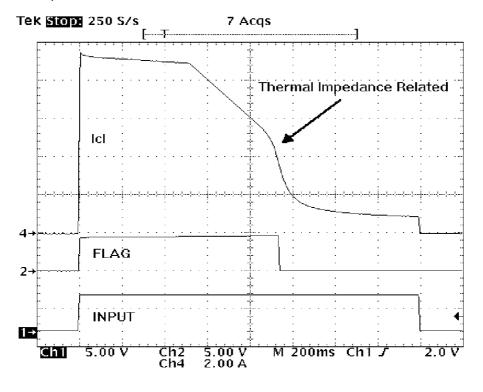
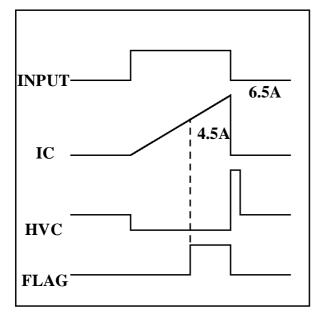


FIGURE 5: Waveforms



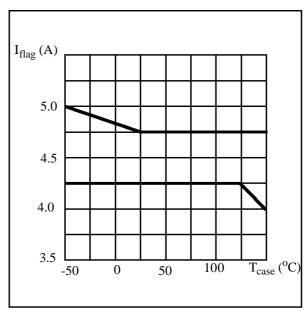
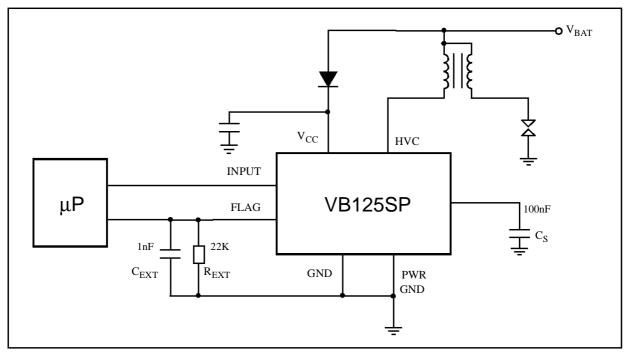


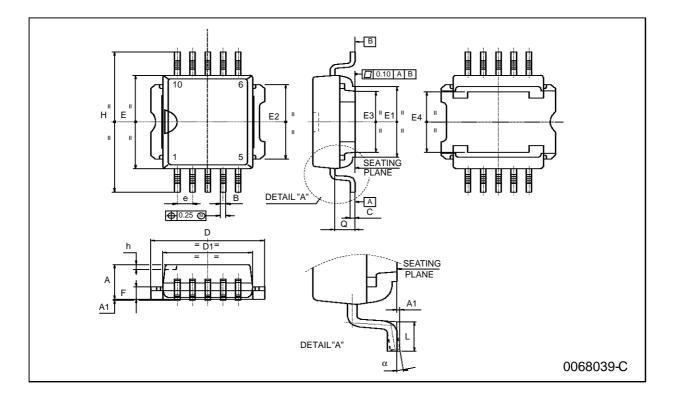
FIGURE 6: Flag Current Versus Temperature

FIGURE 7: Application Circuit



DIM.		mm		inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
В	0.40		0.60	0.016		0.024
С	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
е		1.27			0.050	
F	1.25		1.35	0.049		0.053
Н	13.80		14.40	0.543		0.567
h		0.50			0.002	
L	1.20		1.80	0.047		0.071





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